

WE CLAIM:

1 1. A field effect device, comprising:

2 a crystalline Si body of one conductivity type;

3 a SiGe layer epitaxially disposed on said Si body;

4 a Si layer epitaxially disposed on said SiGe layer; and

5 a source and a drain comprising SiGe in an epitaxial relation with the Si body and
6 connected to each other by the SiGe layer and the Si layer, the source and the drain
7 having a conductivity type opposite to that of the Si body and each forming a
8 heterojunction and a metallurgical junction with the Si body, wherein the heterojunction
9 coincides with the metallurgical junction with a tolerance of less than about 10nm.

1 2. The device of claim 1, wherein the tolerance is less than about 5nm.

1 3. The device of claim 1, wherein the Si body is disposed on top of an insulating layer.

1 4. The device of claim 3, wherein the insulating layer is SiO₂.

1 5. The device of claim 1, wherein the Si body conductivity is n-type, and wherein a hole
2 device current is confined predominantly in the SiGe layer.

1 6. The device of claim 5, wherein the hole device current is directed along one of a <100>
2 or a <110> crystallographic direction.

1 7. The device of claim 1, wherein the Si body conductivity is p-type, and an electron
2 device current is confined predominantly in the Si layer.

1 8. The device of claim 1, wherein the SiGe layer and the SiGe in the source and the drain
2 are compressively strained.

1 9. The device of claim 1, wherein the SiGe layer is between about 5nm and 15nm thick.

1 10. The device of claim 1, wherein the SiGe layer has a Ge concentration which
2 substantially equals a Ge concentration in the SiGe in the source and the drain.

1 11. The device of claim 10, wherein the Ge concentration in the SiGe layer is between
2 about 15% and 50%.

1 12. The device of claim 1, wherein the device has a top surface plane, and wherein the
2 source and the drain are raising above the top surface plane.

1 13. The device of claim 1, wherein the device has a top surface plane that lies essentially
2 in one of a (100), (110) or (111) crystallographic plane.

1 14. The device of claim 1, wherein the source and the drain further comprise an epitaxial
2 Si cap layer disposed on top of the strained SiGe, wherein the Si cap layer is between
3 about 2nm and 30nm thick.

1 15. The device of claim 1, wherein the Si body conductivity is n-type, and the device is
2 connected in a complementary circuit configuration with a field effect device comprising:
3 a crystalline Si body of p-type conductivity;
4 a SiGe layer epitaxially disposed on the p-type Si body;
5 a Si layer epitaxially disposed on the SiGe layer; and
6 a source and a drain of n-type conductivity comprising SiGe in an epitaxial
7 relation with the p-type Si body and connected to each other by the SiGe layer and the Si
8 layer, the source and the drain each forming a heterojunction and a metallurgical junction
9 with the p-type Si body, wherein the heterojunction coincides with the metallurgical
10 junction with a tolerance of less than about 10nm.

1 16. The device of claim 1, wherein the Si body conductivity is n-type, and the device is
2 connected in a complementary circuit configuration with a field effect device comprising:
3 a crystalline Si body of p-type conductivity;

1 a SiGe layer epitaxially disposed on the p-type Si body;
2 a Si layer epitaxially disposed on the SiGe layer; and
3 a source and a drain of n-type conductivity comprising SiGe in an epitaxial
4 relation with the p-type Si body and connected to each other by the SiGe layer and the Si
5 layer.

6 17. The device of claim 1, wherein the Si body conductivity is n-type, and the device is
7 connected in a complementary circuit configuration with a field effect device comprising:

8 a crystalline Si body of p-type conductivity;
9 a SiGe layer epitaxially disposed on the p-type Si body;
10 a Si layer epitaxially disposed on the SiGe layer; and
11 a source and a drain of n-type conductivity connected to each other by the SiGe
12 layer and the Si layer.

1 18. The device of claim 1, wherein the Si body conductivity is n-type, and the device is
2 connected in a complementary circuit configuration with an NMOS device.

1 19. A PMOS field effect device, comprising:

2 a crystalline Si body of n-type conductivity;
3 a SiGe layer epitaxially disposed on the n-type Si body;

1 a Si layer epitaxially disposed on the SiGe layer; and
2 a source and a drain of p-type conductivity comprising SiGe in an epitaxial
3 relation with the n-type Si body and connected to each other by the SiGe layer and the Si
4 layer, the source and the drain each forming a heterojunction and a metallurgical junction
5 with the n-type Si body, wherein the heterojunction coincides with the metallurgical
6 junction with a tolerance of less than about 10nm.

1 20. The device of claim 19, wherein the tolerance is less than about 5nm.

1 21. The device of claim 19, wherein the Si body is disposed on top of an insulating layer.

1 22. The device of claim 21, wherein the insulating layer is SiO₂.

1 23. The device of claim 19, wherein the SiGe layer is between about 5nm and 15nm
2 thick.

1 24. The device of claim 19, wherein the SiGe layer has a Ge concentration of between
2 about 15% and 50%.

1 25. The device of claim 24, wherein the Ge concentration in SiGe layer substantially
2 equals a Ge concentration in the SiGe in the source and the drain.

1 26. A method for producing a field effect device comprising the step of:

2 fabricating a source and a drain by epitaxial deposition of a first material, wherein
3 the first material forms a heterojunction with a second material, and wherein the second
4 material constitutes a body of the device.

1 27. The method of claim 26, further comprising the step of:

2 providing a channel between the source and the drain, wherein the channel
3 consists essentially of the first material.

1 28. The method of claim 26, further comprising the step of:

2 providing a channel between the source and the drain, wherein the channel
3 consists essentially of the second material.

1 29. The method of claim 26, further comprising the step of:

2 providing the body with one conductivity type and providing the source and the
3 drain with an opposing conductivity type forming a metallurgical junction between the
4 body and the source and the drain, and wherein the heterojunction and the metallurgical
5 junction coincide with a tolerance of less than about 10nm.

1 30. The method of claim 29, wherein the body conductivity is selected one of n-type or p-
2 type.

- 1 31. The method of claim 27, wherein the first material is selected to be SiGe and the
2 second material is selected to be Si.
- 1 32. The method of claim 31, wherein the body is selected to be a Si layer on an insulator.
- 1 33. The method of claim 31, wherein in the epitaxial deposition the SiGe is selected to be
2 in one of an undoped state or a p-doped state.
- 1 34. The method of claim 31, wherein in the epitaxial deposition the SiGe is selected to
2 have a Ge concentration of between about 15% and 50%.
- 1 35. The method of claim 31, wherein the SiGe channel is selected to be between about
2 5nm and 15nm thick.
- 1 36. The method of claim 26, further comprising the step of capping the first material with
2 an epitaxial layer of the second material having a thickness of between about 2nm and
3 30nm.
- 1 37. The method of claim 26, wherein the device has a top surface plane and the source
2 and the drain are fabricated to raise above the top surface plane.

1 38. A processor, comprising:

2 at least one chip, wherein the chip comprises at least one field effect device, and

3 wherein the at least one field effect device comprise:

4 a crystalline Si body of one conductivity type;

5 a SiGe layer epitaxially disposed on the Si body;

6 a Si layer epitaxially disposed on the SiGe layer; and

7 a source and a drain comprising SiGe in an epitaxial relation with the Si body and
8 connected to each other by the SiGe layer and the Si layer, the source and the drain

9 having a conductivity type opposite to that of the Si body and each forming a

10 heterojunction and a metallurgical junction with the Si body, wherein the heterojunction

11 coincides with the metallurgical junction with a tolerance of less than about 10nm.